Abstract

The present invention provides a semiconductor memory device for reducing power consumption by turning off a DLL clock tree in stand-by mode. The synchronous semiconductor memory device in accordance with the present invention includes a clock synchronization means for synchronizing a data output with a external clock; and a clock tree on/off control means for delaying an enable timing of a RAS idle signal for a predetermined time after a row inactive instruction is supplied, turning on/off a clock tree of the clock synchronization means in response to the RAS idle signal.